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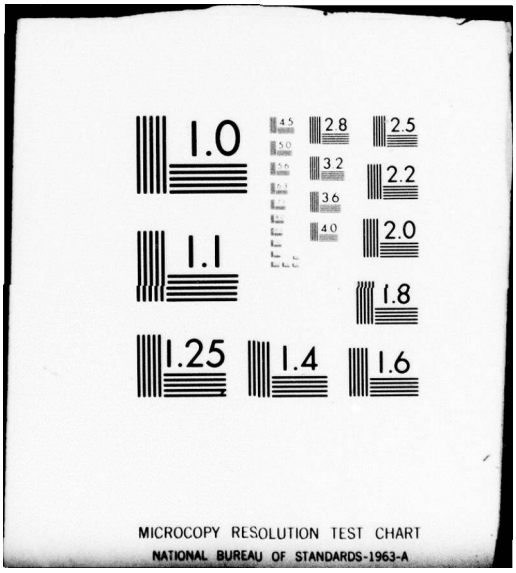
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Technical Document 258

TIME-ENCODED SPATIAL DISPLAY

Time-compressed display system uses solid-state components and data compression techniques for image processing, storage, and retrieval

BD Directo
RJ Morin

25 April 1979

Prepared for
Naval Sea Systems Command
(NAVSEA 652)
Washington DC 20362

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AN ACTIVITY OF THE NAVAL MATERIAL COMMAND

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METRIC CONVERSION

To convert from	to	Multiply by
° (angle)	radians (rad)	1.75×10^{-2}
miles	kilometres (km)	1.609
yards	metres (m)	9.144×10^{-1}

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This report describes in detail the operation and capabilities of the TIESPAD unit, ~~developed at NOSC, San Diego.~~ This unit was tested with an AN/SPS-10 surface search radar and an AN/SPS-30 air search radar, ~~both located on Point Loma, San Diego~~, and with an AN/FPS-93 air search radar ~~on San Clemente Island~~ via a microwave relay, ~~to Point Loma.~~ These brief tests show that the TIESPAD unit does effectively help the operator to detect and track moving targets that would otherwise not be detected on a standard AN/SPS-type indicator.

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OBJECTIVES

The primary objective of this task was to design and develop an improved time-compressed display system that uses solid-state components and data compression techniques for image processing, storage, and retrieval. Secondary objectives included designing capabilities for accepting standard five-wire radar synchro data and for driving standard TV monitors.

The technical and functional suitability of our engineering model of TIESPAD will be evaluated by the Naval Research Laboratory.

CONTENTS

INTRODUCTION

This report documents the development of TIESPAD (Time-Encoded Spatial Display), which is a new concept for a Time-Compressed Display System (TICODS). The report describes the operation of TIESPAD and updates the work described in NOSC Technical Note NELC TN 3173, Preliminary Design for a Modularized Image Processor with Optional Time Compressed Display Capability, 11 June 1976.

The TIESPAD concept evolved from data compression studies for the image processing, storage, and retrieval improvement task funded under Project N431. Preliminary studies under that project dealing with run length coding and delta modulation techniques of data compression were found to be inapplicable to TICODS. It was recognized, however, that in TICODS there is a significant degree of frame-to-frame redundancy. The concept which emerged from this analysis of data compression possibilities in TOCODS is discussed below.

Essentially, TICODS records the events occurring in a defined space over a period of time. If the space is subdivided into small cells and the data in each cell are time-coded, a significant reduction in memory can be realized. Specifically, in TICODS each successive spin of the antenna steps the write frame counter and generates a command to store the events which occurred on the last scan. The existing TICODS design provides for storing 32 scans (frames) in bulk storage; a 4-bit coding is used for video level. If this 32-frame history were to be retained, it could be packed into 16 data frames by using an extra bit in each data frame to indicate block 1 (frames 1-16) or block 2 (frames 17-32). (This method of reducing memory size could be carried further, and the returns from "n" antenna scans could be recorded in memory, provided that $\log_2(n)$ bits are included in addition to the normal 4-bit video data for coding or tagging the time of entry. But we determined that even 32 antenna scans were more than were needed, and we subsequently dropped our storage requirement to 16 frames.) Other possibilities for data compression also became apparent and were implemented as described below.

The design we adopted contains a matrix of 512 × 512 display cells. The TIESPAD memory accommodates video, frame tag, and history bits for each cell, thereby eliminating the bulk memory required in the original TICODS. The video word (4 bits) represents the greatest value of video during the past 16 scans or frames, the frame word (4 bits) provides a time reference for the last time of entry, and the history word (4 bits) records the number of consecutive scans in which an event occurred. In decoding these bits, the start time for the event is taken as frame minus history (F - H) and the end time is frame (F). The decode circuit simply unblanks the video at each display cell when the read frame count falls between these time limits.

Figures 1 and 2 are simplified block diagrams of the original TICODS and TIESPAD, respectively. These figures are intended to illustrate functional differences only; they are not to be construed as representing physical modules. In figure 2, for example, the functions of the write frame block as well as the frame and history encoder block are physically incorporated in a single module called the frame and history encoder. It should also be noted that TICODS records 32 frames of history; whereas TIESPAD, with its solid-state approach, records only 16 frames.

A TIESPAD equipment incorporating the features described in this report has been developed and briefly tested with an AN/SPS-10 surface search radar and an AN/SPS-30 air search radar, both located on Point Loma, San Diego, and with an AN/FPS-93 air search radar located on San Clemente Island via a microwave relay to Point Loma. Test results

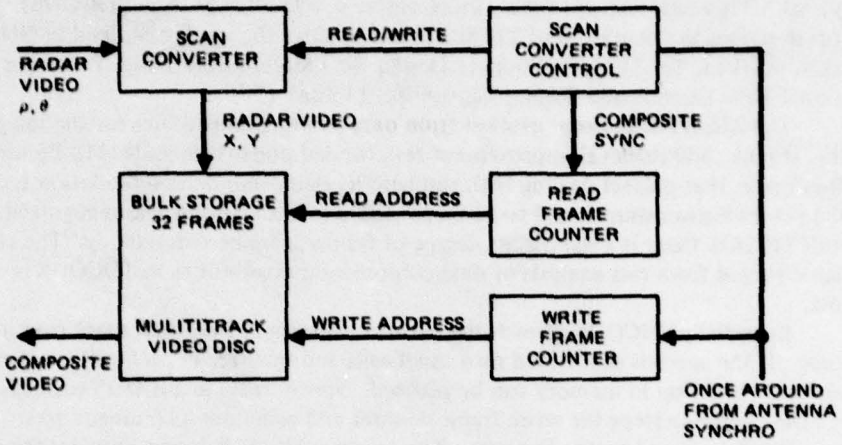

Figure 1. Simplified TICODS block diagram.

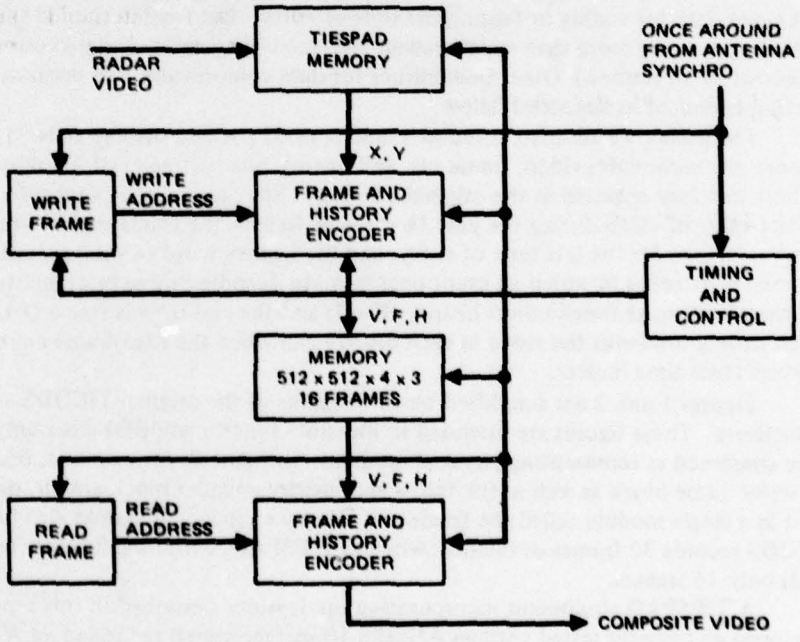

Figure 2. Simplified TIESPAD block diagram.

showed that TIESPAD does effectively help the operator to detect and track moving targets. The TIESPAD unit has been shipped to the Naval Research Laboratory for further test and evaluation.

OPERATION AND CONTROLS

This section describes the function of the various controls and indicators on the TIESPAD control panel (fig 3). Since this equipment was designed for test purposes, several control features were included specifically for test flexibility. The front panel of a unit designed for operational use would be tailored to the needs of operational personnel rather than test personnel.

MODE SELECT. This rotary switch controls the operation of the scan converter in one of eight modes: CONT STORE, LAST SCAN, FREEZE, VARIABLE DECAY, ONES, ZEROS, TEST, and TIESPAD. The first seven modes are really conventional scan converter modes (without time compression) because the frame and history data in the memory are not utilized.

The CONT STORE (continuous store) mode provides continuous mapping of incoming radar video into memory. This generates an infinite buildup of target tracks and noise in the display. Accordingly, this mode displays trails on all moving targets.

The LAST SCAN mode displays a 360° PPI picture of video stored during only the last antenna rotation. This mode includes a continuous update feature by mapping the new video into memory and erasing the old video.

The FREEZE mode provides the ability to store and retain the PPI picture without erasing any data in memory. New video is inhibited from being loaded into memory.

The VARIABLE DECAY mode simulates the persistence decay characteristic of standard radar indicators by periodically reducing the video level code in all 256k display cells by one step. The DECAY RATE potentiometer on the control panel may be adjusted so as to cause the trails on all moving targets to fade in the desired manner.

The ONES mode forces the input video word to an all-ones condition, thereby creating a bright screen. This is provided only as a test feature.

The ZEROS mode forces the input video word to an all-zeros condition, thereby creating a dark screen. This is also provided as a test feature and as a means for clearing all stored video data.

The TEST mode enables the system for manual access and loading of data into any address in the memory. This mode is used with the RUN/TEST switch, MAN STROBE switch, TEST VIDEO, TEST HISTORY, TEST FRAME, Y ADDRESS, and X ADDRESS.

The TIESPAD mode enables the encoding and decoding of frame and history data and displays a time-compressed picture for the last 16 antenna scans. This mode features the dynamic display of all moving targets by sequentially unblanking the display cells along the target's track.

RANGE SELECT. This rotary switch provides nine discrete mileage range scales: 2, 4, 8, 16, 32, 64, 128, 256, and 512.

VIDEO GAIN. This potentiometer provides an adjustment for setting the video brightness.

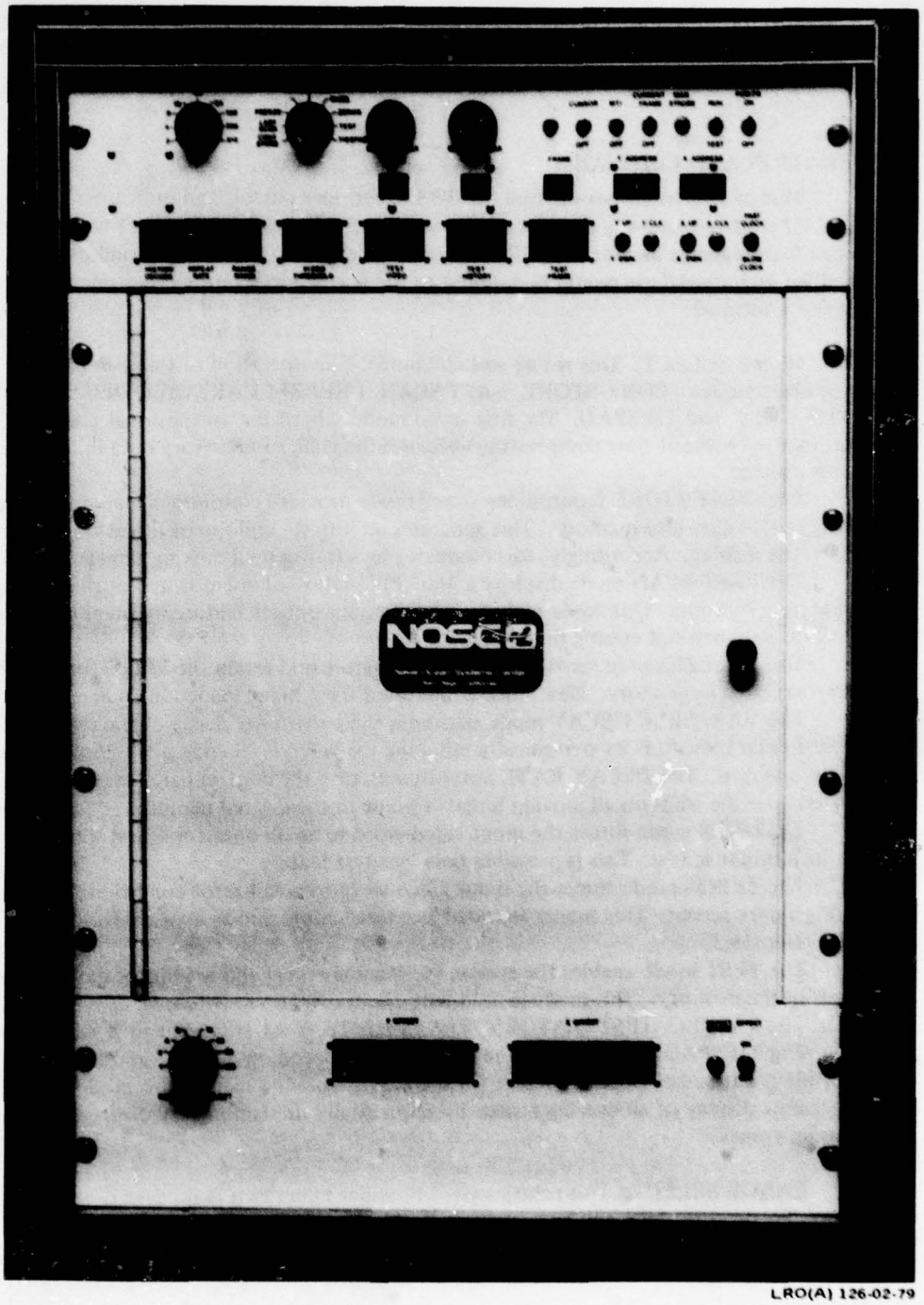

Figure 3. TIESPAD front view, showing controls and indicators.

DECAY RATE. This potentiometer, which is connected to the decay rate oscillator on the address select module, controls the rate of persistence decay.

CURSOR/OFF. This switch enables the display of the X and Y cursors.

MTI/OFF. This switch enables the blanking of display cells with large history values, as in the case for landmass and clutter, to provide a pseudo moving target indicator (MTI) display. A history threshold from the HISTORY DECODE switch provides the reference level for this blanking feature. When the MTI switch is in the MTI position, the display cells are blanked out where the history value is greater than the history threshold.

Display cells with history less than the threshold are unblanked in the normal timed sequenced manner. When the MTI switch is in the OFF position, the display cells with history greater than the threshold will be unblanked in a nonflashing manner, and those with history less than the threshold are unblanked in the timed sequenced manner.

CURRENT FRAME/OFF. This switch, which functions only in TIESPAD mode, enables the continuous display of last target positions. Thus, as viewed by the operator, the target trails are sequentially displayed (but current positions are continuously displayed).

MAN STROBE. This momentary switch generates a clock pulse for manually writing test data into main memory.

RUN/TEST. This switch selects the test address when in the TEST position and selects the sweep address when in the RUN position. The selected address is then used as the write address during memory write cycles.

POWER ON/OFF. This switch applies power to the unit. On turn-off, a slight delay is used for turning off the +5 volt supplies to accommodate the power supply sequencing circuit.

HISTORY DECODE. This lever switch controls the history threshold level used with the MTI feature. The history threshold level is equal to 2 times the HISTORY DECODE number, plus 1. These history threshold settings are 1, 3, 5, 7, 9, 11, 13 and 15.

REPEAT RATE: This lever switch controls the frequency of playback on the 16 frames of history. This ranges from 16 frames in 0.53 second to 16 frames in 8.53 seconds.

RANGE RINGS. This lever switch controls brightness of the range rings in eight steps, including one off position.

VIDEO THRESHOLD. This control provides selectable adjustment of the threshold level for processing video signals and noise. Two lever switches are used to select one of 16 levels (shades of gray) as the video threshold.

TEST VIDEO. This control provides a manual input for video data by means of two lever switches, which select one of 16 levels (gray shades) as the video input word.

TEST HISTORY. This control provides a manual input for history data by means of two lever switches, which select one of 16 history values as the history input word.

TEST FRAME. This control provides a manual input for frame data by means of two lever switches, which select one of 16 frame numbers as the frame input word.

Y UP/Y DOWN. This switch controls the direction of movement for the Y cursor. When it is in the Y UP position and the Y CLK switch is depressed, the Y cursor moves toward the top of the display. When it is in the Y DWN position and the Y CLK switch is depressed, the Y cursor moves toward the bottom of the display.

Y CLK. This switch enables the movement of the Y cursor.

X UP/X DOWN. This switch controls the direction of movement for the X cursor. When it is in the X UP position and the X CLK switch is depressed, the X cursor moves toward the right of the display. When it is in the X DWN position and the X CLK switch is depressed, the X cursor moves toward the left of the display.

X CLK. This switch enables the movement of the X cursor.

FAST CLOCK/SLOW CLOCK. This switch controls the speed of movement for the X and Y cursors. It provides two different clock frequencies to the X and Y cursor counters.

RANGE RING SELECT. This rotary switch provides 8 discrete range ring mileage intervals: 1, 2, 4, 8, 16, 32, 64, and 128.

OFFSET ON/OFF. This switch enables the display to be offset from center. When it is in the OFF position, the display origin is centered in both horizontal and vertical directions. When it is in the ON position, the display origin is offset from center as controlled by the Y OFFSET, X OFFSET, and OFFSET STROBE settings.

Y OFFSET. These lever switches provide the control of the 17-bit Y offset word, which is set up by setting the octal-coded lever switches to the proper offset address, then entering this word into the Y address generator module. The actual entry of the offset word is controlled by the OFFSET STROBE switch and the OFFSET ON/OFF switch.

X OFFSET. These lever switches provide the control of the 17-bit X offset word, which is set up in the same way as the Y offset word.

OFFSET STROBE. This momentary switch clocks the X and Y offset words into data latches on the X and Y address generator modules. However, this signal is generated only when the OFFSET ON/OFF switch is in the ON position.

VIDEO. This indicator displays the numerical value of the video data stored in memory at the address for the intersection of the X and Y cursors. This indicator requires the RUN/TEST switch to be in the TEST position to send data from memory. The indicator is disabled when the switch is in the RUN position.

HISTORY. This indicator displays the history data stored in memory in the same manner as for VIDEO.

FRAME. This indicator displays the frame number stored in memory in the same manner as for VIDEO.

Y ADDRESS. This indicator displays the octal-coded address for the Y cursor. It is disabled when the RUN/TEST switch is in the RUN position and it is enabled when that switch is in the TEST position.

X ADDRESS. This indicator displays the octal-coded address for the X cursor. It is controlled in the same manner as for the Y ADDRESS.

FUNCTIONAL DESCRIPTION

The function of the Time-Encoded Spatial Display (TIESPAD) unit is to record and display radar target history and to generate a time compressed display for enhancing target detection and tracking. This is accomplished by the use of a solid-state scan converter with expanded memory and processing functions for recording the time of last hit and the duration of events at each display cell. The scan converter architecture can be divided into the following major functions:

Analog-to-digital conversion
Address generation
Address selection
Sweep data store
Frame and history encode
Main memory store
Frame and history decode
Digital-to-analog conversion
Timing and control

ANALOG-TO-DIGITAL CONVERSION

This function includes limited analog processing of the radar video input signal, followed by quantization of the video into 4-bit digital words. Each 4-bit word represents one of 16 gray shades. The analog processing includes dc restoration, gain control, peak detection and low-pass filtering.

ADDRESS GENERATION

This function generates the "sweep addresses" for mapping the incoming radar data into the memory. This is done in several steps because of the retention of a preliminary design for a Naval Tactical Data System (NTDS) interface and the modification necessary for interfacing to a standard five-wire radar synchro. Address generation includes

Synchro-to-digital angle conversion
Digital angle-to-sine/cosine conversion
Delta X/delta Y pulse train generation

X/Y address generation

X/Y offsetting

Range scaling

Off-screen detection

ADDRESS SELECTION

This function time multiplexes display addresses and sweep addresses during read and write memory cycles. Read cycles are conducted on a cycle-stealing basis during the active TV line time. This provides a continuous display with noninterrupted, real-time updating.

SWEEP DATA STORE

This function provides the interface between the fast data transfer rate of the incoming radar data and the slow data processing rate of the memory. This requires two high-speed prememories for alternately receiving and transmitting the video/address data associated with one radar sweep.

FRAME AND HISTORY ENCODE

This function compares incoming video data with past events at each display cell and selects one of eight processing states as dictated by the TIESPAD algorithm. Each processing state is a particular condition which can be detected to enable the appropriate video, scan, and history data to be loaded back into memory. The action taken for each processing state is shown in table 1.

State 1 is a "new hit" condition on a moving target. The conditions for this state are a strong video signal exceeding the video threshold, no previous hits during the current frame, and no saturated history. Peak video, current frame, and incremental history are loaded into memory when this state is selected.

State 2 is a "multiple hit on same frame" condition. The conditions are similar to State 1 except that the old frame number is the same as the current frame number. This indicates that there was a previous hit during the current frame; therefore the history should not be incremented. Peak video, current frame, and old history are loaded into memory when this state is selected.

State 3 is a "landmass" condition because of the saturated history value. Since the largest value for history is 15, further hits on the landmass or clutter cannot exceed this saturated value. Peak video, current frame, and old history are loaded into memory when this state is selected.

State 4 is a status quo condition, with all video in the current scan below video threshold and with the current frame not yet advanced to the start position, F – H. In this state no new information is stored; instead, old video, old frame, and old history are loaded into memory.

State 5 is a "no hit history decrement" condition. The difference between this state and State 4 is that now the current frame has wrapped around the 16 frame numbers and is at the start frame time. Since there is no strong video signal and the start frame time is now

Table 1. TIESPAD processing routines.

Processing State	Input Conditions				Data Into Memory		
1 New hit	NV ≥ T	CF ≠ F	H ≠ 15		PV	CF	H + 1
2 Multiple hit/same frame	NV ≥ T	CF = F	H ≠ 15		PV	CF	H
3 Landmass/saturated history	NV ≥ T		H = 15		PV	CF	H
4 Status quo	NV < T	CF ≠ F - 0	H ≠ 0		OV	F	H
5 No hits history decrement	NV < T	CF = F - 0	H ≠ 0		OV	F	H - 1
6 No hits/erase video	NV < T	CF = F	H = 0		NV	CF	H
7 No hits/old noise	NV < T	CF ≠ F	H = 0	NV < OV	OV	F	H
8 No hits/new noise	NV < T	CF ≠ F	H = 0	NV ≥ OV	NV	CF	H

Legend:
- NV – New video
- T – Video threshold
- CF – Current frame number
- F – Old frame number
- H – Old history number
- OV – Old video
- PV – Peak video

16 frames old, it is time to drop the last frame. Therefore, old video, old scan, and decremented history are loaded into memory. The latter input causes the last frame to be dropped from memory.

State 6 is a "no hit/erase video" condition. The difference between this state and State 5 is that the old history value is now zero. Since there is still a weak video signal, this new video word is loaded into memory, thereby erasing the old video. Current frame and a history value of zero are loaded into main memory.

State 7 and State 8 are for processing weak video signals and noise. As shown in table 1, State 7 retains the old video and old frame since the new noise value is less than the old noise value. State 8 stores the new video and current frame since the new noise value is greater than or equal to the old noise value. The result of both states is to retain the peak value of noise and the time of occurrence. The significance of these two states is that noise will appear as a random pattern on the display, whereas the weak target will follow a continuous path.

MAIN MEMORY STORE

This function provides the long-term storage of video, scan, and history data. This requires a memory capacity of 256k × 12 for the TIESPAD mode and a memory capacity of

256k X 4 for the simpler scan converter modes. Memory addressing is partitioned into 512 X addresses and 512 Y addresses. Memory cycle times and display addressing are synchronized to the TV raster.

FRAME AND HISTORY DECODE

This function decodes the frame and history data from memory and enables the display of the video data in a sequential manner. The replay and repeat rate for the 16 frames of history are selectable from the control panel. A pseudo-MTI and a current track feature are provided for enhancing the detection and tracking of fast moving targets.

DIGITAL-TO-ANALOG CONVERSION

This function converts the digital video, cursor, sync, and blank into a composite video signal for driving a standard TV monitor.

TIMING AND CONTROL

This function synchronizes all other functions to the TV raster. It generates all the control signals for memory. It controls the transfer of data out of the prememories. It generates the RS-170 TV sync signals and the display addresses to read data out of main memory for display on the TV raster.

THEORY OF OPERATION

The following paragraphs describe the theory of operation for the 12 types of TIESPAD modules. A schematic diagram is included for each module. Figure 4 is an overall system block diagram showing the module interconnections. (Fig 4-23 are placed at the end of this document to aid continuity.)

SYNCHRO-TO-ΔX/ΔY MODULE

This module (fig 5, 6) receives an 11-bit azimuth word from the synchro-to-digital converter and generates sine and cosine modulated pulse trains corresponding to the change in position along the radar sweep. The nine least significant bits (LSBs) of the azimuth word define an angle between 0° and 90° and are used for addressing the sine and cosine look-up tables. The two most significant bits (MSBs) of the azimuth word define the quadrant and are used to invert the 9-bit azimuth word during quadrant fold-over, to provide full 360° coverage.

The cascaded look-up tables convert the 9-bit azimuth input into 16-bit binary values of sine and cosine. Each 16-bit word is latched into storage registers at the start of each radar sweep. These 16-bit sine and cosine words are then used to control the rate of pulse generation by the cascaded rate multipliers for the ΔX and ΔY pulse trains.

The inputs to the rate multipliers include the 16-bit rate word, a 10.237 MHz gated clock (CK), and an enable signal ($\overline{EN}$). The rate multipliers are preset with the rate word during radar dead time and are enabled for generating pulse trains at the start of the radar

sweep. Each ΔX or ΔY pulse represents a change in position of about 16 yards. The resulting ΔX and ΔY pulse trains are buffered via line drivers, U29A and U29B, for distribution to the X and Y address generator modules.

Sign ΔX and sign ΔY are generated to indicate the direction of travel along the respective X and Y axes. These signals are derived from the two MSBs of the 11-bit azimuth word by detecting the sweep quadrant (U19B, U19C and U19D). Both signals are buffered for distribution to the X and Y address generator modules. Also, sign ΔY is used on the frame and history encoder module to generate a "once around" pulse for indicating a 360° rotation of the radar antenna.

Another function on this module is a power supply controller for sequencing the turn-on and turn-off of the dc power supplies (−15, −5, +5, +12 and +15 volts). This controller energizes the power supplies in the following sequence: the +5 volt supplies; the triple supply of −5/−15/+15 volts; the +12 volt supply. The turn-off sequence is done in reverse order. This sequence is used to protect the MK 4116 memory chips, which might be damaged if the 12 volt supply were applied first.

ANALOG-TO-DIGITAL MODULE

This module (fig 7) conducts limited analog processing and converts the radar video signal into a 4-bit digital word. The analog processing includes dc restoration, gain control, peak detection, and low-pass filtering. The dc restorer circuit is located on the back of the control panel near the video gain potentiometer, R5A. This circuit clamps the baseline of the video signal to signal ground via Q1A and CR1A. Gain control is provided via potentiometer R5A.

A 2.5× inverting amplifier is included to match the full-scale input range of the analog-to-digital converter. The output of the amplifier is buffered by U2 and sampled by the peak/average detector. The voltage on storage capacitor C7 is buffered by U3 and converted into a digital word on control of the start-of-conversion (SOC) pulse. The voltage on C7 is reset by the end-of-conversion (EOC) pulse.

The 4-bit video word represents one of 16 gray shades. A 3-bit range mark word is added to the 4-bit video word via NOR gates U8A, U8B, U8C, and U8D. The resulting video word is then buffered for distribution to the prememory modules.

SWEEP TIMING CONTROL MODULE

This module (fig 8) generates the sweep timing signals, sampling strobes, and range marks for controlling the radar interface module set: synchro-to-ΔX/ΔY module, analog-to-digital module, X and Y address generator modules, and prememory modules. Sweep timing consists of the following synchronizing signals: start-of-sweep (SOS), end-of-sweep (EOS), load counters (LC), and prememory select (SEL). These signals synchronize the generation of sweep addresses and the conversion of radar video with the start of each radar sweep.

SOS is generated by the leading edge of radar trigger and indicates the beginning of a new radar sweep. This control signal is used to clear the range counter (U30, U42, U41, U40, and U29), to clear the "LC" flip flop (U5A), and to latch the sine/cosine words into storage registers.

EOS is generated approximately 100 microseconds before the next SOS pulse. This is done by storing the maximum range count between consecutive SOS pulses, then detecting

the range count that occurs about 100 microseconds before the maximum range count. The EOS pulse is used to preset the "LC" flip flop (U5A).

The output of the "LC" flip flop (U5A) is a 100-microsecond LC pulse that occurs during radar dead time. This pulse is used to toggle the "SEL" flip flop (U5B), to preset the address counters on the X and Y address generator modules, and to reset the rate multipliers on the synchro-to-$\Delta X/\Delta Y$ module.

The output of the "SEL" flip flop (U5B) controls the time multiplexing operation of the two prememory modules and the selection of prememory write enable (PM$\overline{WE}$) strobes. Prememory write enable strobes are generated from either end-of-conversion (EOC) or prememory read/write (PM $\overline{R}$/W). They reflect the different data rates during alternate radar sweeps.

Start-of-conversion (SOC) is initiated whenever the sweep changes position in the display matrix. This pulse is generated by a change in the LSB of either the 9-bit X or 9-bit Y sweep address. The SOC pulse initiates one conversion cycle for the analog-to-digital module. It also latches the X/Y sweep addresses into pipeline registers (U16, U17, and U18), and latches the range mark amplitude into storage register U9.

ADDRESS GENERATOR MODULES

There are two identical address generator modules (fig 9, 10): A4 generates the X sweep address; A5 generates the Y sweep address. Both address generator modules operate in parallel and identically.

The purpose of these modules is to receive the $\Delta X/\Delta Y$ clocks, to generate a 17-bit address count, and to provide a range-scaled 9-bit sweep address. The $\Delta X/\Delta Y$ pulse train and sign $\Delta X/\Delta Y$ are buffered for controlling a 17-bit address counter. This counter consists of five cascaded up/down binary counters (U4, U5, U6, U7, and U8). The other inputs to this counter are a load counter (LC) strobe and a 17-bit offset word.

The 17-bit address counter is preset to the offset coordinate by the LC strobe during radar dead time. The LC strobe enables the address counter to start counting at start-of-sweep. $\Delta X/\Delta Y$ clocks the address counter and sign $\Delta X/\Delta Y$ controls the up/down direction of counting. The resulting 17-bit address word is buffered and distributed to the range scaling and off-screen detection circuits.

Range scaling generates a 9-bit sweep address from the 17-bit address count. This is done by selecting the appropriate group of 8 bits from the address counter's 16 LSBs. The address counter MSB is always used as the sweep address sign bit. This data selection process is done in two stages to accommodate the nine different range scales.

Off-screen detection is accomplished by examining the unused bit field between the address counter's MSB and the selected range scale's eight bits. If all the bits in this field are identical and equal to the inverted MSB, an on-screen flat is generated.

For example, on a 32-mile range scale, the following selection will occur:

Buffered counter outputs A4 to AA1 will be selected for the XO/YO to X7/Y7 sweep address LSBs.

Buffered counter outputs AS will be selected for the XS/YS sweep address MSB.

Buffered counter outputs A12 to A15 will be examined for a matched condition with $\overline{AS}$. If a matched condition occurs, an on-screen flat is generated.

An off-screen condition from either the A4 or A5 module will cause the range scaling data selectors (U34 and U35) to output a zero sweep address for both X and Y.

PREMEMORY MODULES

There are two identical prememory modules (fig 11, 12) that operate in a time multiplex mode. These modules provide temporary storage for the incoming radar data and transfer the data out upon demand by the memory timing. Each prememory module contains a 1024 X 22 bit bipolar memory, a 10-bit address counter, and two groups of data selectors. These two modules operate alternately: as one receives incoming data, the other transmits outgoing data. Just before the start of the next sweep, the modules exchange operations so that the receiving module becomes the transmitter and the transmitting module becomes the receiver.

The 10-bit address counter is cleared by the LC strobe during radar dead time, and is clocked by the prememory write enable (PM$\overline{\text{WE}}$) clock. The 10-bit address is heavily buffered to drive the 22 bipolar memory chips.

The two groups of data selectors are divided into input selectors and output selectors. The input selectors select incoming radar data for data storage during receive operations and select "zero" data during transmit operations. The output selectors conduct the multiplexing of the prememory outputs for the memory. The outgoing video data are transmitted to the frame and history encode module, and the outgoing sweep addresses are sent to the address select module.

ADDRESS SELECT MODULE

This module (fig 13, 14) generates an 18-bit test address for manual operations, conducts the time multiplexing of sweep, display and test addresses into a 7-line address bus, and provides the control for a persistence feature with a variable decay rate.

An 18-bit test address is generated by two 9-bit counters: X cursor counter and Y cursor counter. Each counter is independently controlled by use of two toggle switches on the control panel: X CLK/Y CLK and X UP (Y UP)/X DWN (Y DWN). This test address provides manual access and entry of data into any area of memory.

The time multiplexing process is done in several steps. The first step is to select a write address from either the sweep address inputs or from the cursor counters. This write address is used during memory write cycles for randomly accessing one memory cell.

The second step is to interweave display addresses with the write addresses during read and write memory cycles. The display address is used to read 16 consecutive memory cells during each read cycle. This block transfer is done 32 times during each TV line. Therefore, only 14 bits of addressing are required during these read cycles. The last step of address multiplexing is required to format the 14-bit memory address onto the 7-line address bus. This is done by dividing the memory address into a 7-bit row word and a 7-bit column word. Inverting line drivers are provided for distributing the address bus to the 12 memory modules.

The 4 LSBs of the write address are multiplexed with a 4-bit persistence address and are buffered for distribution to the memory modules. This 4-bit address is decoded on each memory module for generating a write enable strobe to the appropriate RAM chip. The persistence address is selected only during persistence erase cycles. This occurs when the scan converter is operated in the variable decay mode. The normal read cycles are converted

into read-modify-write cycles, and the video level at each display cell is decreased by one gray shade. This process takes 16 TV frames (0.53 second) to access the 256k display cells and to decrease the screen brightness by one gray shade.

TIMING AND CONTROL MODULE

This module (fig 15, 16) synchronizes the operation of all other modules with the timing of the TV raster. A crystal oscillator produces a 20.475 MHz master clock for clocking the TV sync generator and for advancing the 11-bit horizontal position counter. The horizontal line time is locked to this frequency such that 1300 clock pulses are counted per horizontal line. Various control signals are generated by detecting specific counts or count multiples along the horizontal line. Each memory cycle is 16 clock periods long and each horizontal line is divided into 81 full memory cycles.

The end-of-line signal indicates the last full memory cycle in the horizontal line and clears the horizontal position counter just before the start of the next line. Flip-flop U46A is cleared at count 1296, then is set by the leading edge of horizontal drive.

The read enable signal enables the time multiplexing of read and write addresses and enables the stealing of memory cycles for read cycles. *Flip-flop U46B is set at count 236,* then is cleared at count 1260.

The read cycle signal steals memory cycles for read operations. The first 15 memory cycles in each horizontal line are dedicated to write operations. The first read cycle starts at count 240 and lasts for the next 16 counts. This is followed by alternating write and read cycles till the end of line. There are 32 read cycles during each horizontal line.

The shift/load and shift clock signals control the block transfer of data from the memory into parallel-to-serial shift registers. First a block of 16 words is read out of memory and loaded into the shift register. Then the words are shifted out at a serial data rate of 10.237 MHz. The first load command occurs at count 256 and is repeated every 32 counts. There are 32 shift/load pulses during each horizontal line.

The read/write address select signal controls the time multiplexing of read and write addresses. Flip-flop U27A is toggled every 16 counts beginning at count 236.

The display blank signal enables the display of video during active line time for 1024 counts and blanks out the display during the remaining time. Flip-flop U27B is set at count 256 and cleared at count 1280. This signal also enables 512 shift clock pulses to be generated during this time.

The prememory output transfer flip-flop controls the transfer of data from the prememories to the memory. The load strobe (LD STB) signal clocks the prememory outputs into data latches on the address select module and on the frame and history encode module. The LED strobe (LED STB) clocks memory data into the LED indicators on the control panel.

Row address strobe (RAS), row/column address select (RW/$\overline{\text{CM}}$), column address strobe (CAS), latch strobe (Lat STB), and write enable (WE) are generated during each memory cycle for synchronizing the read-modify-write functions within the 781-nanosecond cycle time. Write enable is inhibited during read cycles and is enabled during write cycles and persistence erase cycles. Figure 17 shows a typical 16-count memory cycle. RAS goes active low at count 0 and initiates the start of a memory cycle. It also strobes the 7-bit row address into each 16k RAM chip. Then, on count 1, the row/column address select puts the 7-bit column address into the address bus. CAS goes active low at count 3 and strobes the 7-bit column address into each 16k RAM chip. At this time, since $\overline{\text{WE}}$ is in a read state, data appear at the 16k RAM output after the 135-nanosecond access time. These

data are strobed into buffer registers by latch strobe at count 6. This completes the read portion of the memory cycle. The next 195 nanoseconds are dedicated for data processing during the modify portion of the memory cycle. The write portion starts with $\overline{WE}$ going active low at count 10. Data into the 16k RAM chip must be stable for the next 55 nanoseconds to insure that the correct data are strobed into memory. Lastly, at count 13, $\overline{RAS}$, $\overline{CAS}$, RW/$\overline{CM}$, and $\overline{WE}$ are reset in preparation for the next memory cycle.

Another function of this module is to generate the X/Y display address and to detect its coincidence with the X/Y test address. The Y display address is generated by an 8-bit counter and a set-clear flip-flop. The flip-flop, U32B, generates the Y address LSB, YRO, by detecting odd-field or even-field pulses from the TV sync generator. The other Y address bits are generated by counting horizontal drive pulses in each TV field. This counting process is delayed 5 lines after the trailing edge of vertical drive to provide a vertically-centered display.

A Y cursor coincidence pulse is generated when the 9-bit Y display address is identical to the 9-bit Y test address. This coincidence pulse is used in the video sum module for unblanking a horizontal cursor on the TV display.

The X display address is generated by subtracting an offset value from the horizontal position count. The resulting 5-bit address is sent to the address select module. The X cursor coincidence pulse is generated by comparing the outputs of the X position counter with the 9-bit X test address. This coincidence pulse is used for unblanking a vertical cursor on the TV display.

FRAME AND HISTORY ENCODER MODULE

This module (fig 18, 19) contains the input processing circuits for encoding the TIESPAD data. This requires comparing the new data with past history at each display cell, then determining the condition of eight possible states:

State 1. A new hit

State 2. A multiple hit on same frame

State 3. Landmass/saturated history

State 4. Status quo

State 5. No hits/history decrement

State 6. No hits/erase video

State 7. No hits/old noise

State 8. No hits/new noise

Each state requires that a specific type of video, frame, and history data be loaded back into memory. All this processing is done during the 195-nanosecond modify time of each write cycle.

New video is received from prememory A and latched into register U7, where it is stored for the full 781-nanosecond memory cycle. This new video is compared with the video threshold word to determine whether a target or noise is at the display cell. This new video is also compared with the old video from memory to determine the largest value of video between the two words.

Each 360° revolution of the radar antenna generates via the sync-to-$\Delta X/\Delta Y$ module a once-around pulse that increments a 4-bit current frame counter. The once-around pulse

occurs as the radar antenna swings across the +X axis from the first to the fourth quadrant. The current frame count provides a time reference for all hits occurring in one 360° rotation of the antenna. The current frame count is compared with the old frame number to determine whether there is a "multiple hit" condition or a "no hit/erase video" condition. The current frame count is also compared with the start frame number (F – H) to determine whether there is a "no hit/history decrement" condition.

Meanwhile, during the 195-nanosecond modify time of each write cycle, old video, frame, and history data are received from memory via buffer drivers U24, U25, and U13. This 12-bit data word represents the past history at the display cell and is modified before loading data back into memory.

When the MODE SELECT switch is in any of the simple scan converter modes, the TIESPAD processing routines are disabled and the selection of processed video is controlled from the control panel. When the MODE SELECT switch is in the TIESPAD position, the video select gates are controlled by the processing states and not by the video select code from the control panel.

The video selectors (U12, U11, U10, and U9) select one of six types of video data for writing into memory: peak video, new video, old video, decremented video, zero video, and test video. Peak video is the larger value between the old video and the new video. Decremented video is selected during persistence erase cycles and is generated by subtracting one gray shade from the old video. Zero video is used to clear the video portion of memory. Test video provides the means for manual entry of video data into memory.

The frame selectors (U51, U52, U39, and U40) select one of three types of frame data for writing into memory: current frame, old frame, and test frame. Current frame represents the new frame number associated with the last hit.

The history selectors (U53, U54, U41 and U42) select one of six types of history data for writing into memory: old history, zero history, history of 1, incremented history, decremented history, and test history. Incremented history is generated by adding a value of one to the old history. Decremented history is generated by subtracting a value of one from the old history.

TV SYNC DRIVER MODULE

This module (fig 20) contains the level shifting and driver circuits for generating RS-170 TV sync signals for use by other TV processing equipment. This requires translation of 0 volt and +5 volt signal levels to –4 volt and 0 volt signal levels, respectively. In addition, these 4 volt sync signals must have enough drive to appear across a 75 ohm load impedance with a source impedance of 75 ohms. These four TV sync signals are horizontal drive, vertical drive, composite sync and composite blank. Each output signal is wired to a BNC connector on the right side panel.

FRAME AND HISTORY DECODER MODULE

This module (fig 21) contains the output processing circuits for decoding the TIESPAD data. The 4-bit read frame counter, U13, provides the time reference for replaying the 16 frames of history and provides for a repeat rate that is selectable at the control panel. The video at a display cell is unblanked only when the read frame count is within the start frame (F – H) and last frame (F) limits. Otherwise, the video is blanked out when the read frame count is outside these limits and during retrace times.

The on frame enable signal controls the unblanking of video by enabling the video gating circuits (U6A, U6B, U7A, and U7B). This enable signal is generated when the read frame count falls into one of three brackets: inside bracket, outside bracket, and zero history. The inside bracket condition is used when F is greater than H such that the start frame, F – H, is a positive number. The outside bracket condition is used when F is less than H such that the start frame is a negative number. And the zero history condition is used when H = 0.

The module also provides for a moving target indicator (MTI) mode by recognizing that large history values are related to very slow or stationary targets. Therefore, landmass and clutter can be eliminated by blanking out the video that corresponds with history values above a history threshold. This history threshold is controlled by the HISTORY DECODE lever switch on the control panel. U16 compares the history data with the history threshold and outputs an enable pulse for the on frame and MTI enable gates.

When the MODE SELECT switch on the control panel is in any of the simple scan converter modes, the TIESPAD decoding circuits are disabled and the video data are always allowed thru the video gating circuits, unaffected by the on frame detect and MTI enable gates.

VIDEO SUM MODULE

This module (fig 22) converts the 4-bit video words into an analog signal, mixes in X cursor and Y cursor, mixes in composite sync and composite blank, and buffers the composite video signal. Adjustable gain controls are provided for setting the cursor, sync, and blank levels. An 8-bit digital-to-analog converter is used in this 4-bit configuration to yield the full output swing of zero to +1 volt.

X cursor coincidence and Y cursor coincidence are mixed via NOR gate U2A. A CURSOR (on/off) switch is located on the control panel for enabling the display of X and Y cursors.

MAIN MEMORY MODULE

Each memory module (fig 23) contains a 256k X 1 RAM array, a 4-to-16 line decoder, a 16-to-1 line data selector, and a 16-bit parallel-to-serial shift register. On-board buffering is provided for distribution of addresses and strobes to each of the 16 RAMs. In addition, buffer registers are included to latch the data from the RAM outputs.

During memory write cycles and persistence erase cycles only one memory cell is read out and written into. The 4-bit X address selects one of the 16 RAM chips for sending data out, then generates an active write enable pulse to that selected RAM chip for writing data in.

During memory read cycles, the outputs from all 16 RAM chips are loaded into the 16-bit shift register. This shift register is clocked by a 10.237 MHz clock and is loaded once every 16 clock pulses. No write enable signals are generated for this memory cycle.

SUMMARY

This report describes in detail the operation and capabilities of the TIESPAD unit, developed at NOSC, San Diego. This unit was tested with an AN/SPS-10 surface search radar and an AN/SPS-30 air search radar, both located on Point Loma, San Diego, and with an AN/FPS-93 air search radar on San Clemente Island via a microwave relay to Point Loma. These brief tests show that the TIESPAD unit does effectively help the operator to detect and track moving targets that would otherwise not be detected on a standard AN/SPS-type indicator. (See figures 24-28.)

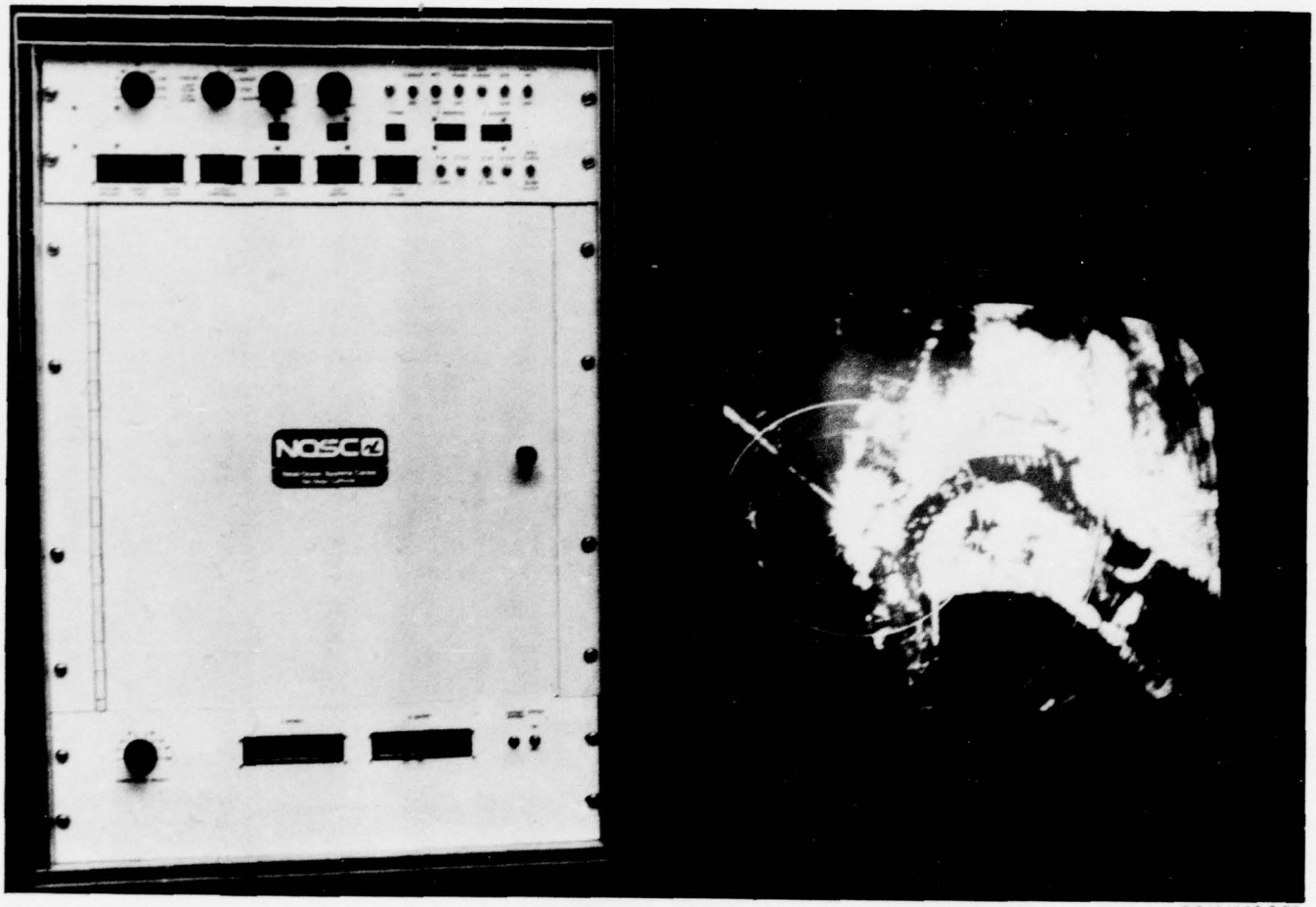

Figure 24. TIESPAD and display.

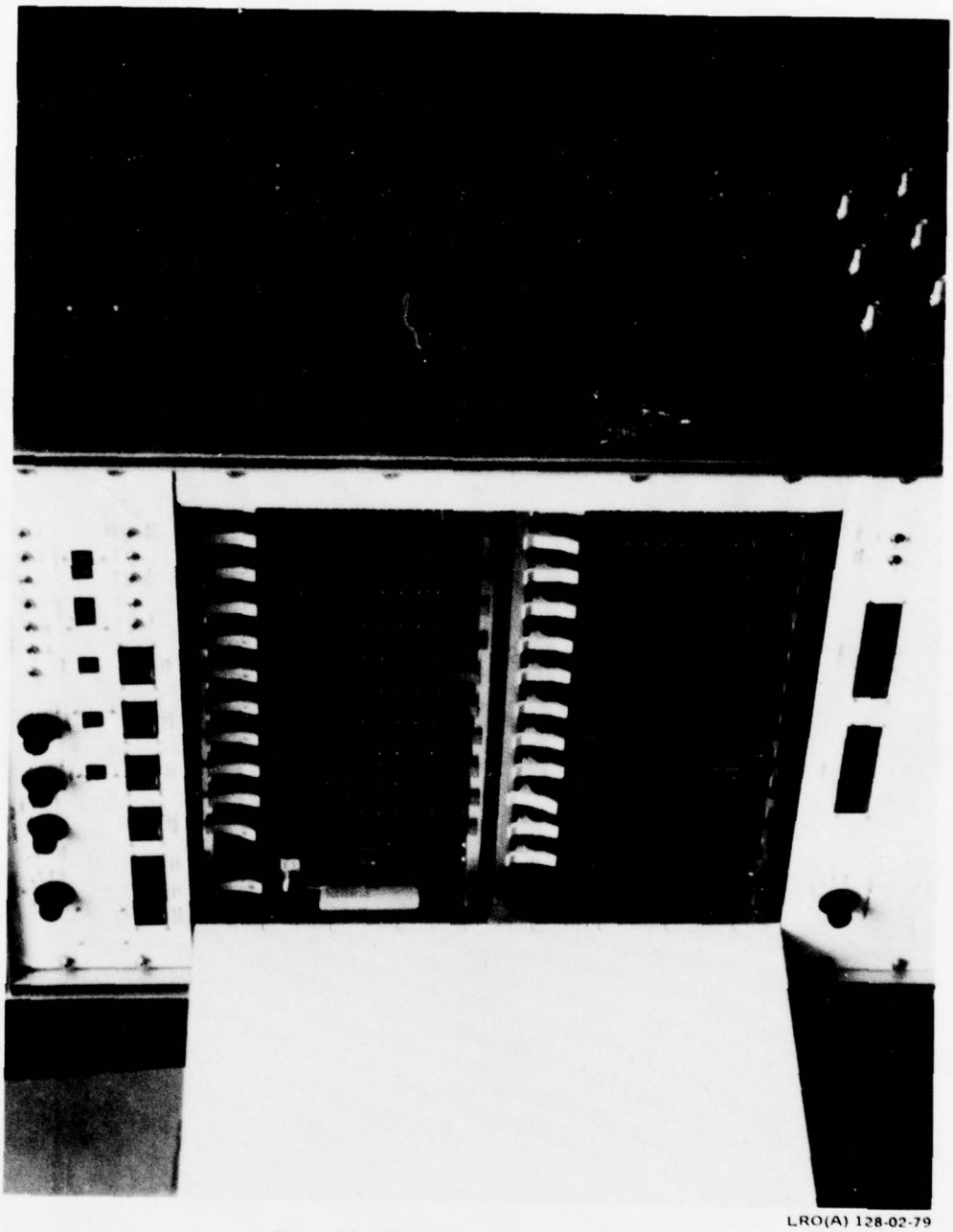

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Figure 25. TIESPAD with front door open.

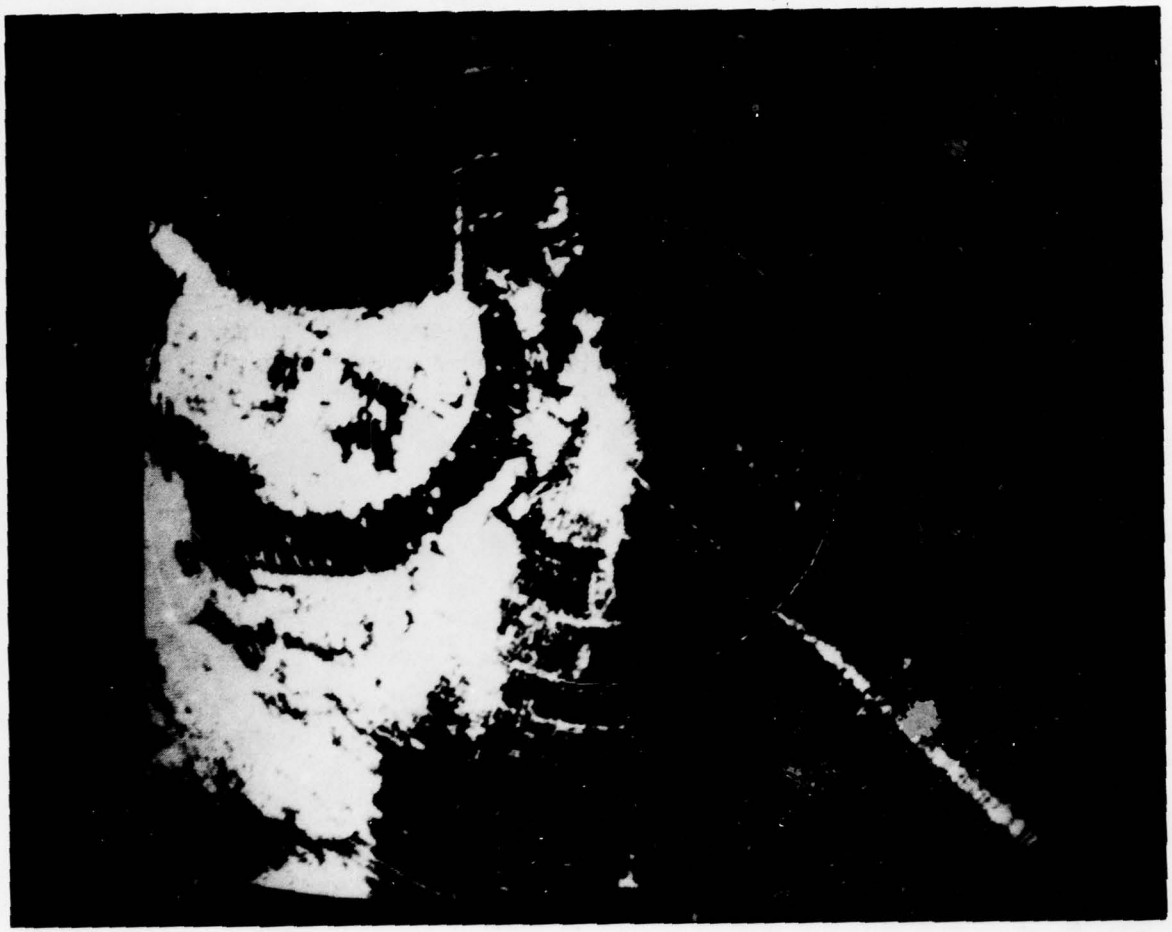

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Figure 26. Display of SPS-10 radar (Point Loma), last scan mode, 4-mile range.

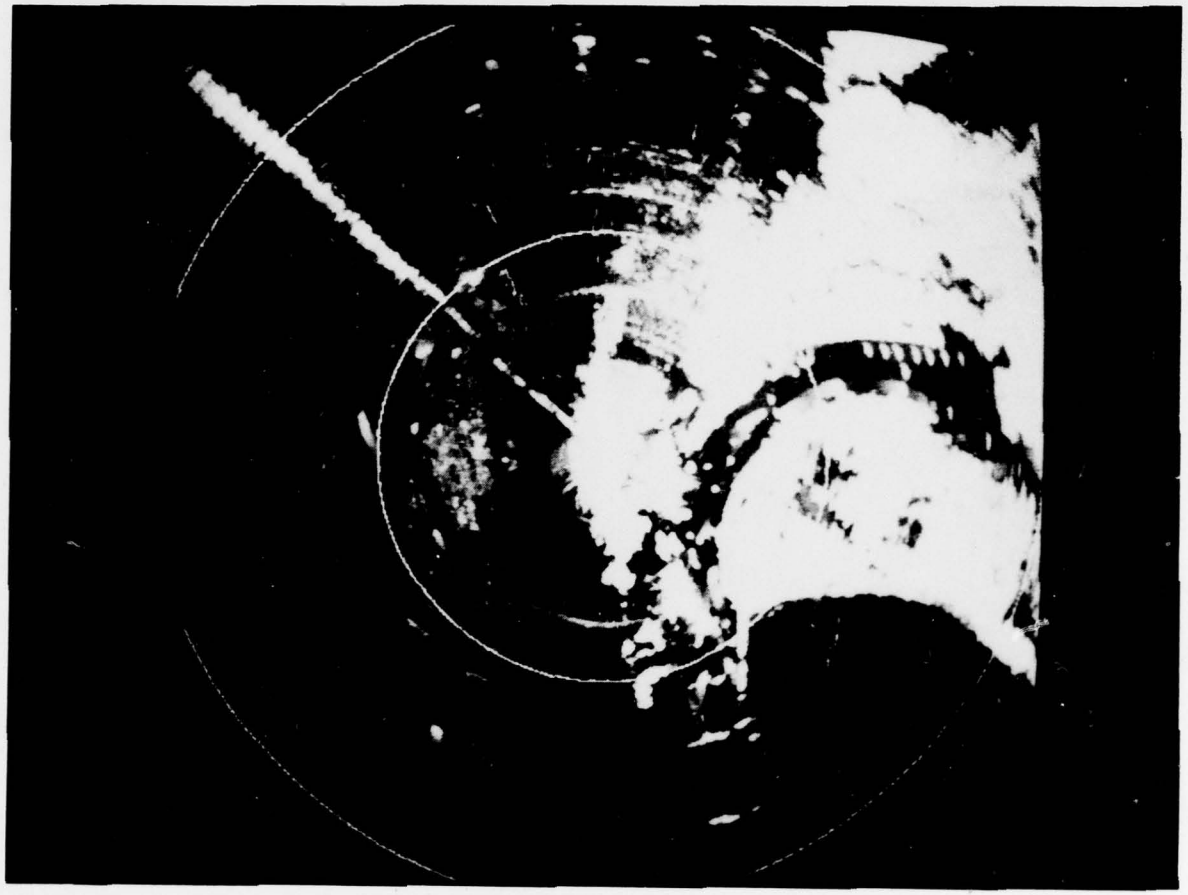

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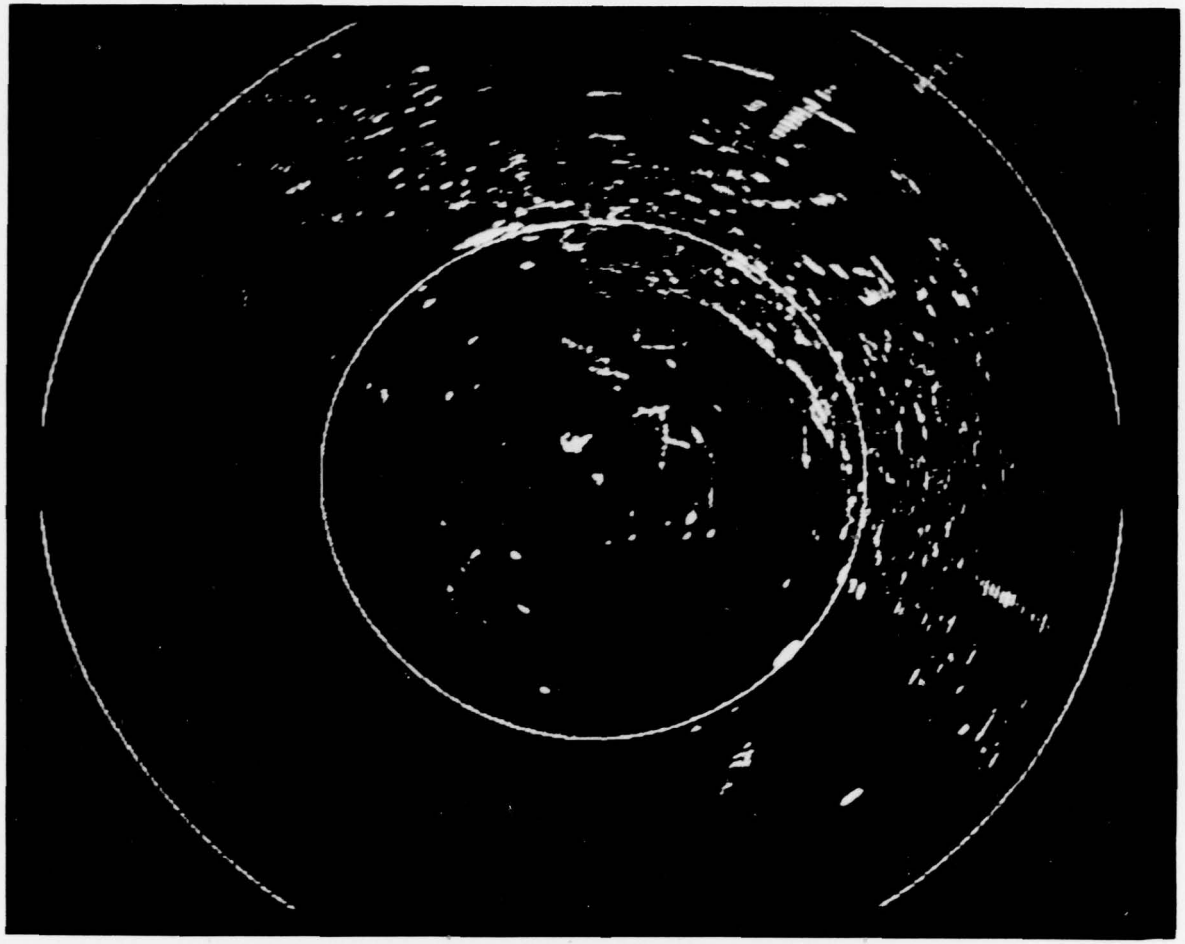
Figure 27. Display of SPS-10 radar (Point Loma), long decay mode, 4-mile range.



LRO(A) 130-2-79

Figure 26. Display of FPS-93 radar (San Clemente), MTI mode, 128-mile range.